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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,583	01/15/2004	Axel K. Kloth	022150-2.00US	8008

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EXAMINER	
TSAI, TSUNG YIN	
ART UNIT	**PAPER NUMBER**
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,583	KLOTH, AXEL K.	
	Examiner	Art Unit	
	Tsung-Yin Tsai	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawing

1. The following drawings are objected and need the following correction:

(1) Figure 7, part 410. Re-label the term "PCI-X or 3GIO Card" outside the figure 410. It is confusing if the label is for part 410 or just for the box below it.

(2) Figure 7, part 410. Label the figure labeled "Realignment Unit & Frame Buffer" as part 412. There is no label for this figure, but the specification label the box as part 412 (page 9 line 24).

(3) Figure 7, part 420. Re-label the term "Host Motherboard" outside the figure of 420. It is confusing if the label is for part 422 or for the part 420, in this way we will know that part 420 is the "Host Motherboard."

(4) Figure 7, part 422. There are multipart numbers assign to the same part. Part 422 is also label as part 416 in the specification (page 9 line 25). Please be consistence with the labeling by changing **ONE** of the following:

- On figure 7 re-label figure 422 as figure 416 to be consistence to the specification **OR**
- Page 9, line 25, change "host DRAM 416" to "host DRAM 422" to be consistence to figure 7.

Please make the following correction. No new matters are allow.

Specification

2. The disclosure is objected to because of the following informalities:

(1) Page 8, line 20, where cited "As shown in Fig. 7" replace with "As show in Fig. 6" such that reading the specification it will be pointing to the correct figure that is in discussion.

(2) Page 9, line 24, where cited "frame buffer 412, one **ore** more IPE 200, and one **ore** More PPE 500." Replace with "frame buffer 412, one **or** more IPE 200, and one **or** More PPE 500."

(3) Page 9, line 28, where cited "one **ore** more ADCs." Replace with "one **or** more ADCs."

Claim Rejections – 35 USC 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juvinall (US Patent Number 5,214,713. IDS) in view of Chen et al (US Patent Number 5,535,288).

Juvinall disclose an image processing system comprising:

(1) Regarding claim 1:

an image processing engine (48 figure 1, column 10 lines 3-23) adapted to perform object-independent processing corresponding to a first layer (48 figure 1) of the image processing system, said image processing engine further adapted

to include a plurality of processors (column 10 lines 6-15) each associated with a different one of pixels of the image frame (column 10 lines 3-23. The CCD array is seen as the first layer that has the plurality of processors sensors that process incoming analog signal to become each pixels.);

a post processing engine adapted to perform object-dependent processing corresponding to a second processing layer of the image processing system (52 figure 1, figure 2, 80-86 figure 4, column 1 lines 25-40, column 10 lines 3-27 and 50-67), and

a processing engine adapted to perform object composition, recognition and association corresponding to a third processing layer of the image processing system (column 4 lines 45-64. Image processing algorithms perform the object composition, recognition and association; seen as the third image processing layer.).

Juvinall does not disclose the said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1; post-processing engine in detail, wherein, Chen et al further provide the details for the post-processing engine.

However, Chen et al disclose a post processing engine adapted to perform object-dependent processing corresponding to a second processing layer of the image processing system, said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having

disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1 (figures 5-7, columns 7-9. The figures show the layout of the post-processing engine in hardware format. The post-processing engine is the second layer because it the obtaining data what has been taken already, but not process. Columns 7-9 describe how the data will be process by the post-processing engine.)

It would have been obvious to one skill in the art at the time of the invention to employ Chen et al teachings to Juvinall to clarify the design of the post-processing engine. In doing so, the design structure of this post-processing engine provides the optimal use of computation (column 7 lines 15-20) as well as performing two simultaneous 2-dimensional cross correlations of data sets (column 8 lines 7-10).

(2) Regarding claim 2:

Juvinall further disclose the plurality of processors of the image processing engine form a massively parallel processing system (94-96 figure 5, column 7 lines 53-67 to column 8 lines 1-24. The parallel processing system is describe.).

(3) Regarding claim 3:

Juvinall further disclose the massively parallel processing system is a systolic array type massively parallel processing system (84-86 figure 4, 94-96 figure 5, column 2 lines 55-60. Where the system is in a systolic array matrix type format.).

(4) Regarding claim 4:

Juvinall further disclose the systolic array type massively parallel processing system is configured as a single-instruction multiple-data system (column 2 lines 60-67, column 3 lines 45-63. Single-instruction system is describe.).

(5) Regarding claim 5:

Juvinall further disclose each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time (column 9 lines 3-45, column 9 lines 24-30. A dimension for the image format is described as being process one after another, suggesting the passage of time.).

(6) Regarding claim 6:

Juvinall further disclose an image capturing block (48 figure 1, 48 figure 3, 76 figure 4, column 1 lines 29-33, column 2 lines 46-49, column 1 lines 66-67, column 10 lines 3-24. A camera and/or CCD are presented in the invention.).

(7) Regarding claim 7:

Juvinall further disclose the plurality of processors are formed on a first semiconductor substrate different from a second semiconductor substrate on which the image capturing block is formed (column 6 lines 64-67 to column 7 lines 1-17. CCD and/or camera is couple to the interface that has the plurality of processor, thus they are all on different substrates.).

(8) Regarding claim 8:

Juvinall further disclose a realignment buffer adapted to realign the data received from first and second analog-to-digital converters disposed in the image capturing block (column 8 lines 48-67 to column 9 lines 1-21. When the systolic array of processors request data, the main processor will alignment the buffer with data using FIFO method to feed the data to the processor matrix.).

Juvinall disclose a method of processing image comprising:

(9) Regarding claim 9:

performing object-independent processing corresponding to a first image processing layer (column 10 lines 3-23. The CCD array is seen as the first layer that has the plurality of processors sensors to deal with each incoming pixels.);

performing object-dependent processing corresponding to a second processing layer (52 figure 1, figure 2, 80-86 figure 4, column 1 lines 25-40, column 10 lines 3-27 and 50-67); and

performing object composition, recognition and association corresponding to a third processing layer (column 4 lines 45-64. Image processing algorithms perform the object composition, recognition and association; seen as the third image processing layer.).

Juvinall does not disclose the post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an

integer greater than 1; post-processing engine in detail, wherein Chen et al further provide the details for the post-processing engine.

However, Chen et al disclose a post processing engine adapted to perform object-dependent processing corresponding to a second processing layer of the image processing system, said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1 (figures 5-7, columns 7-9. The figures show the layout of the post-processing engine in hardware format. The post-processing engine is the second layer because it the obtaining data what has been taken already, but not process. Columns 7-9 describe how the data will be process by the post-processing engine.)

It would have been obvious to one skill in the art at the time of the invention to employ Chen et al teachings to Juvinall to clarify the design of the post-processing engine. In doing so, the design structure of this post-processing engine provides the optimal use of computation (column 7 lines 15-20) as well as performing two simultaneous 2-dimensional cross correlations of data sets (column 8 lines 7-10).

(10) Regarding claim 10:

Juvinall further disclose performing object independent processing by a plurality of processors that form a massively parallel processing system (94-96

figure 5, column 7 lines 53-67 to column 8 lines 1-24. The parallel processing system is describe.).

(11) Regarding claim 11:

Juvinall further disclose the massively parallel processing system is a systolic array type massively parallel processing system (84-86 figure 4, 94-96 figure 5, column 2 lines 55-60. Where the system is in a systolic array matrix type format).

(12) Regarding claim 12:

Juvinall further disclose configuring the systolic array massively parallel processing system as a single-instruction multiple-data system (column 2 lines 60-67, column 3 lines 45-63. Single-instruction system is describe.).

(13) Regarding claim 13:

Juvinall further disclose each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time (column 9 lines 3-45, column 9 lines 24-30. A dimension for the image format is described as being process one after another, suggesting the passage of time.).

(14) Regarding claim 14:

Juvinall further disclose capturing the image frame on a first semiconductor substrate that is different from a second semiconductor substrate on which the plurality of processors are formed (column 6 lines 64-67 to column

7 lines 1-17. CCD and/or camera is couple to the interface that has the plurality of processor, thus they are all on different substrates).

(15) Regarding claim 15:

Juvinall further disclose converting analog data corresponding to the image frame to digital data; and realigning the converted digital data (column 8 lines 48-67 to column 9 lines 1-21. When the systolic array of processors request data, the main processor will alignment the buffer with data using FIFO method to feed the data to the processor matrix. The inherit function of the CCD is to convert analog single to that of digital data in order for the processors to process it.).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pechanek et al (US Patent Number 6,405,185 B1) disclose massively parallel array processor.

Wilkinson et al (US Patent Number 5,713,037) disclose slide bus communication functions for SIMD/MIMD array processor.

Coldren et al (US Patent Number 4,707,647) disclose gray scale vision method and system utilizing same.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsung-Yin Tsai whose telephone number is (571) 270-1671. The examiner can normally be reached on Monday - Friday 8 am - 5 pm ESP.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tsung-Yin Tsai
March 13, 2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER